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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

Application No. : 09/460,898

Filing Date : December 14, 1999

First Named Inventor : N. Matsuoka et al.

Group Art Unit : 2756

Examiner Name :

Attorney Docket No. : FUJY 16.847

Sheet 1 of 1

**U.S. PATENT DOCUMENTS**

Examiner Initials	Cite No. <sup>1</sup>	U.S. Patent Document	Kind Code if known <sup>2</sup>	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns Lines Where Relevant Passages or Relevant Figures Appear
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**FOREIGN PATENT DOCUMENTS**

Examiner Initials	Cite No. <sup>1</sup>	Foreign Patent Document Office <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)	Country	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns Lines Where Relevant Passages or Relevant Figures Appear

**OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), data, page(s), volume-issue number(s), publisher, country, where published, source.	Applicant check here if English language translation attached <sup>7</sup>
C&F		1998 Electronics Information and Communication Society Communication Society Conference, A study on scheduling algorithms for input buffered ATM switches, K. Kawarai, et al., Fujitsu Laboratories Ltd.	RECEIVED MAR 20 2001 Technology Center 2100
C&F		Terabit Switch Architecture using Input Queueing Technique, K. Kawarai et al., Fujitsu Laboratories Ltd.	
C&F		The Institute of Electronics, Information and Communication Engineers, Technical Report of IEICE, A Study on Large Scale Input Queueing Switch Architecture, H. Tomonaga, et al. Fujitsu Laboratories, Ltd.	

Examiner Signature		Date Considered	11/5/02
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